

# Depletion-mode polysilicon optical modulators in a bulk complementary metal-oxide semiconductor process

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We demonstrate depletion-mode carrier-plasma optical modulators fabricated in a bulk complementary metal-oxide semiconductor (CMOS), DRAM-emulation process. To the best of our knowledge, these are the first depletion-mode modulators demonstrated in polycrystalline silicon and in bulk CMOS. The modulators are based on novel optical microcavities that utilize periodic spatial interference of two guided modes to create field nulls along waveguide sidewalls. At these nulls, electrical contacts can be placed while preserving a high optical Q. These cavities enable active devices in a process with no partial silicon etch and with lateral  $p$ - $n$  junctions. We demonstrate two device variants at 5 Gbps data modulation rate near 1610 nm wavelength. One design shows 3.1 dB modulation depth with 1.5 dB insertion loss and an estimated 160 fJ/bit energy consumption, while a more compact device achieves 4.2 dB modulation depth with 4.0 dB insertion loss and 60 fJ/bit energy consumption. These modulators represent a significant breakthrough in enabling active photonics in bulk silicon CMOS—the platform of the majority of micro-electronic logic and DRAM processes—and lay the groundwork for monolithically integrated CMOS-to-DRAM photonic links. © 2013 Optical Society of America

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A central challenge in the continued scaling of massively multicore processors and the realization of the exascale supercomputing paradigm is to reduce processor-to-memory interconnect power consumption while maintaining growth in data bandwidth density. Wavelength-division multiplexed silicon photonic interconnects hold promise as a technology capable of replacing electrical CPU-memory interconnects [1]. To this end, photonic components compatible with advanced logic complementary metal-oxide semiconductor (CMOS) and DRAM processes must be developed. Substantial progress has recently been made in the monolithic integration of photonics in state-of-the-art logic CMOS with no process changes [2,3] and in a modified DRAM peripheral process [4]. However, energy-efficient depletion-mode optical modulators have not been demonstrated in bulk CMOS, DRAM, or any process where the active layer is polycrystalline silicon.

In this Letter, we demonstrate depletion-mode modulators fabricated in a short-flow polysilicon process that emulates a full-flow commercial DRAM process. This DRAM emulation process was subject to many of the constraints of the full-flow process, including the absence of a monocrystalline device layer, partial silicon etch, or vertical  $p$ - $n$  junction implants. In modulator design, a partial etch is commonly employed to form ridge waveguides with electrical contact made to the remaining slab [5–7]. Vertical junctions have been used as an alternative contact geometry compatible with a full silicon etch [8]. Recently, a spoked-ring modulator design was demonstrated that employs radial lateral junctions and is fully compatible with a logic CMOS process [3]. However, this design is not well suited to a memory process with coarser implant mask resolution. In the present work, we introduce a new

type of optical cavity wherein multimodal interference gives rise to optical field minima at waveguide sidewalls where electrical contacts can be placed. Such a design also circumvents the need for either a partial etch or a vertical  $p$ - $n$  junction and is compatible with coarse-resolution implant masks. A schematic of the device is shown in Fig. 1(a). Photonic devices are fabricated in a 220 nm thick polysilicon layer on a 1.2  $\mu\text{m}$  thick, deposited deep trench isolation oxide layer [9] to provide optical

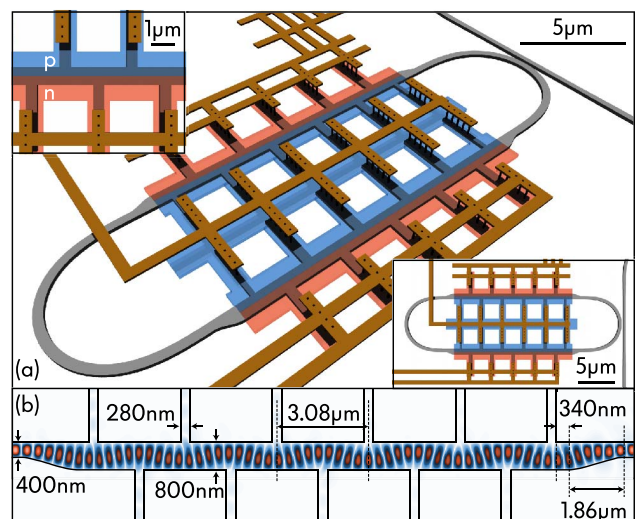


Fig. 1. (a) Layout of 5-period monolithically integrated polysilicon modulator, dual-mode waveguide regions with  $p$ - $n$  junctions, nonadiabatic mode converters, and metal contacts (via height magnified 2 $\times$  for clarity). Left inset, contacts and lateral junction; right inset, top view. (b) Field magnitude,  $|H_z|$ , simulated with finite-difference time-domain (FDTD).

confinement. Nitride and oxide dielectrics are present in the near field of the devices, and a single copper layer contacts the active silicon layer through tungsten plugs. Modulator variants demonstrated here occupy between 300 and 600  $\mu\text{m}^2$  in area. The devices demonstrate that energy-efficient, depletion-mode optical modulators can be made in a polysilicon device layer and are fully compatible with a bulk silicon, including DRAM, process flow, thereby circumventing the need for hybrid integration [10] or modifications to existing bulk CMOS or DRAM [4] process infrastructure. These results mark significant progress toward the realization of monolithic CMOS-to-DRAM photonic links and interconnects.

The optical cavity employed in this device is based on a racetrack-type geometry [11], shown in Fig. 1. The straight waveguide section comprises a single-mode section connected to a dual-mode section by a nonadiabatic taper; electrical contacts are placed in the dual-mode section. The length of the taper is chosen to excite a specific ratio of modes  $\text{TE}_1$  and  $\text{TE}_2$ . The two modes interfere with a beat period given by  $\Lambda = 2\pi/(\beta_1 - \beta_2)$ , and loss is minimized for a certain ratio of amplitudes of the two modes. The resulting field pattern (magnitude) is shown in Fig. 1(b). Contacts are placed periodically, at the field nodes, and are used to drive a  $p$ - $n$  junction that runs down the center of the dual-mode waveguide [Fig. 1(a), left inset]; the voltage across this junction controls the width of the depletion region and therefore, through the carrier-plasma effect, the index of refraction. Time-reversal symmetry ensures that the mirrored taper at the exit of the modulator arm recombines the two modes back into one in the single-mode waveguide, with no loss in principle.

The two straight arms of the racetrack resonator are connected by single-mode,  $180^\circ$  bends with a varying radius of curvature along the bend. These gradual bends transition adiabatically from the straight section (zero curvature) to a circular arc section (local curvature  $1/r$ ). Such bends eliminate junction loss [12] at the straight-to-bend interface and distribute the transition, enabling higher  $Q$  racetrack cavities.

For modulators based on this type of cavity, the number of periods of contacts affects several aspects of device performance including free-spectral range (FSR), resonant frequency shift under drive conditions (related to the fraction of the cavity volume in which carrier density modulation is taking place), and on-resonance extinction for a given coupling gap. We present data taken from a device with 5 periods of contacts (22 total contacts) and one with 15 periods of contacts (62 total contacts). Figure 2(a) shows passive transmission spectra from the two cavities. The 5-period device has a larger FSR and larger on-resonance extinction because of design-rule limited coupling gaps in this design, such that both devices are undercoupled at the realized cavity loss levels. For the same gap, coupling per unit time is stronger in the smaller device. This can be corrected in future designs by lengthening the coupling region or reducing loss. Figures 2(b) and 2(c) show optical micrographs of the two devices under consideration.

For transistors fabricated in polysilicon, high doping levels ( $>10^{19}/\text{cm}^3$ ) are usually utilized. For depletion-mode carrier-plasma modulators, moderate doping

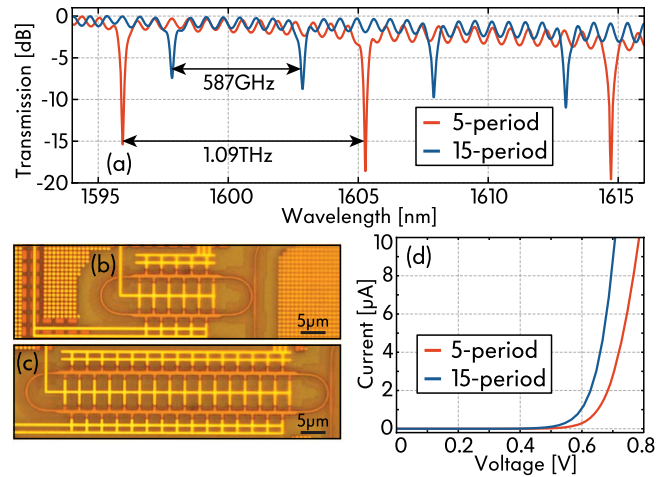


Fig. 2. (a) Optical transmission spectral response of 5- and 15-period devices. (b) and (c) Optical micrographs of the two devices. (d) I-V curves of the modulator diodes.

levels closer to  $10^{18}/\text{cm}^3$  are useful due to the reduced free-carrier absorption and larger depletion region width modulation. However, the activation of dopants as a function of implant concentration is nonunity in polysilicon and is a highly nonlinear function [13]. Hall measurements indicate that activated dopant concentrations were achieved in the ranges  $7\text{--}9 \times 10^{17}/\text{cm}^3$   $n$  type and  $6\text{--}8 \times 10^{17}/\text{cm}^3$   $p$  type. The ranges are due to uncertainty in the carrier mobility. The I-V curve shown in Fig. 2(d) confirms that rectifying junctions were formed in both devices. Optical transmission spectra reveal loaded  $Q$  factors of 5900 and 4300 in the 5- and 15-period devices, respectively. Figure 3(a) shows spectral shifts in the 15-period cavity under DC-bias conditions from  $-3.5$  V to  $0.5$  V.

Figures 3(b) and 3(c) show eye diagrams from the 5- and 15-period devices, respectively. The data were acquired on a sampling oscilloscope with a 20 GHz optical sampling module and 12.4 GHz electrical low-pass filter. The device was driven with a 5 Gbps,  $2^{31} - 1$  bit pseudorandom binary sequence by a 40 GHz ground-signal-ground (GSG) probe. Voltage doubling is expected to occur at impedance mismatch between the  $50 \Omega$  drive line and the modulator diode. Under this assumption, the voltage swing actually seen by the modulator is  $-3.5$  V to  $+0.5$  V. Such a voltage swing is achievable by integrated driver circuits. Under these operating conditions, the 15-period device provided 3.1 dB modulation depth with 1.5 dB insertion loss. Its energy consumption is estimated at 160 fJ/bit [average switching energy,  $(1/4)CV_{pp}^2$  for non-return-to-zero (NRZ) data] using the 0 V junction capacitance at the high end of the dopant concentration range. The 5-period device provided 4.2 dB modulation depth with 4.0 dB insertion loss at a calculated 60 fJ/bit energy consumption. The I-V curve indicates that steady-state driving current contributes negligibly to the energy consumption.

The 15-period device had a larger mode shift under the bias swing because the  $p$ - $n$  junction fills a larger fraction of the cavity and was therefore able to operate with lower insertion loss. However, the 5-period device had a larger on-resonance extinction, allowing for greater modulation depth. Between these two, for an optical link,



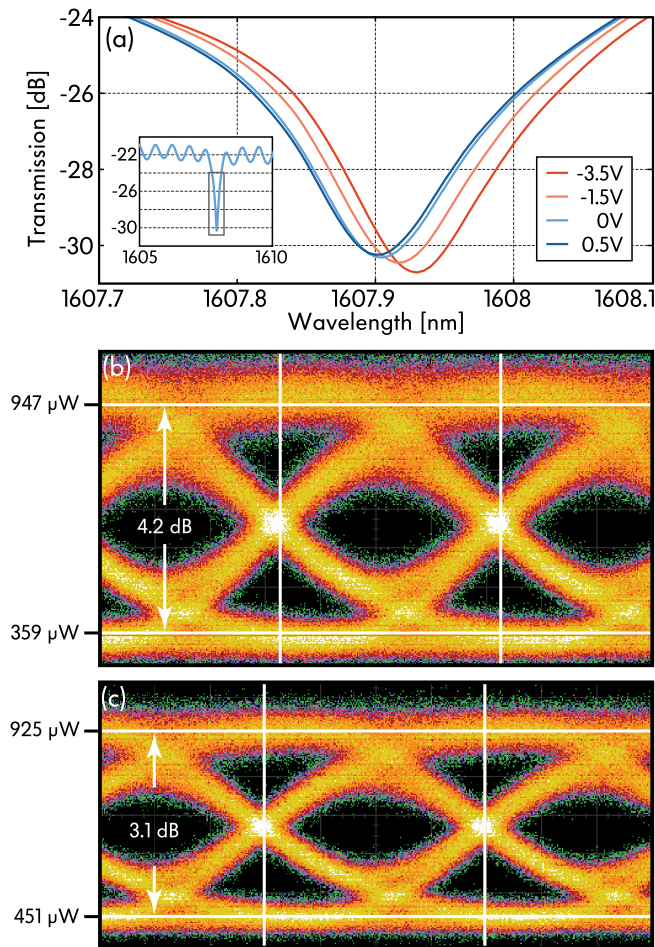


Fig. 3. (a) Near-resonance optical response of the 15-period device at DC bias voltages from  $-3.5$  V to  $+0.5$  V. (b) 5 Gbps optical eye diagram from the 5-period device showing 4.2 dB modulation depth in response to the same voltage swing. (c) 5 Gbps optical eye diagram from the 15-period device with 3.1 dB modulation depth ( $-3.5$  V to  $+0.5$  V voltage swing).

the lower insertion loss device is preferable because laser power enters the energy budget.

Increasing the number of periods of contacts leads to a decreased device resistance but increased capacitance. The  $RC$  time constant is independent of number of periods. The optical loss  $Q$  has also been shown to depend only weakly on the number of periods in an undoped cavity [11]. However, in doped cavities, a larger fraction of the modal fields overlaps the doping, contributing to a reduced loss  $Q$  in the larger cavity. The energy consumption depends only on the capacitance and voltage swing and therefore grows with the number of periods.

In this cavity design, the bend section does not contribute to modulation but does reduce the FSR. It was implemented with a large radius of curvature to ensure low optical loss. Because bending loss is not a significant contributor to the loss  $Q$ , compacting this portion of the optical cavity, by using a tighter radius and optimized curvature profile, can increase the FSR and the mode shift. An ultracompact design could result from using a circular generalization of this multimode cavity design

[14]. Extinction can be improved by calibration of the cavity  $Q$  and use of a distributed coupler where the critical dimension rules limit coupling gap choice.

We believe that this demonstration of a depletion-mode optical modulator in polysilicon on a bulk CMOS memory process is an important milestone toward enabling complete photonic links monolithically integrated with advanced electronics and implemented directly in existing advanced-node bulk CMOS or DRAM foundries.

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