Linear Photonic Crystal Microcavities in Zero-Change SOI CMOS

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Abstract: Linear photonic crystal microcavities are demonstrated in 45 nm SOI CMOS with no process changes in foundry. Side-coupled waveguide excitation decouples cavity and coupling design. A loss Q on the order of 100,000 is demonstrated.

OCIS codes: (230.5298) Photonic crystals; (200.4650) Optical interconnects; (230.4000) Microstructure fabrication.

1. Introduction

Energy-efficiency and bandwidth density requirements in future CPU to memory interconnects and other advanced electronics applications have motivated research into monolithic integration of photonics with microelectronics [1]. Recent design techniques have allowed for photonic devices to be laid out and fabricated within standard process design kit (PDK) guidelines in advanced CMOS processes without requiring any in-foundry process modifications [2–4]. Nanostructured devices such as photonic crystals require the resolution and low proximity effects typical in electron beam lithography [6]. Advanced 45 nm CMOS also permits the resolution and process control to define photonic crystals. Photonic crystal cavities offer important potential building blocks for efficient filtering, tuning, modulation, all optical switching and nonlinear applications [5, 6].

In this paper, we demonstrate efficient linear photonic crystal cavities in a state-of-the-art SOI CMOS process, implemented in the transistor-body device layer. We demonstrate devices with nearly ideal behavior at a loaded Q of 2,150 (92 GHz), and extract a loss Q on the order of 100,000. The cavities are excited via evanescent coupling [8–10], enabling decoupled design of the microcavity and waveguide coupling. Based on this building block, using pairs of cavities, filters with 100% transmission on resonance can be constructed [8], with natural port separation, such as that in microring resonator structures.

2. Design of a photonic crystal microcavity in a standard SOI CMOS process

In this work, we employ the IBM 45nm 12SOI process [11]. Recent work has shown similar cavity designs in a bulk silicon (polycrystalline device layer) process [12]. An advantage of the SOI CMOS process is the low optical loss of the monocrystalline silicon transistor body layer. The silicon device layer is kept undoped using dopant block layers in the process [2]. The primary challenges in design are the sub-90 nm thickness of the body silicon layer which limits confinement and process design rules, including minimum enclosed area and notch rules. This process has a relatively low minimum enclosed area rule which places a strong constraint on the cavity design. As a result, in variants designed for 1200 nm we explored alternative unit cell designs such as isolated rectangles of core material. The cavities presented here use square holes as the unit cells to simplify layout and design rule conformance [2]. The cavity mask was designed in a standard Cadence environment.

The cross-section of the cavity within the 12SOI process is illustrated in Fig. 1(a) (exact layer dimensions available in IBM 12SOI Process Design Kit under NDA [11]). Because of the thin body silicon layer, the cavity waveguide width is large relative to typical designs [6] to maximize confinement [Fig. 1(e)], and the cavity is also longer to support a high radiation Q. Although the polysilicon gate layer could be employed on top of the c-Si body to increase confinement [4], it is omitted because its substantial optical loss would degrade the Q.

The cavity is synthesized to support Hermite-Gaussian resonant modes, i.e. to approximate a truncated parabolic potential, using rigorous numerical band-structure calculations [7]. HFSS (a commonly used RF tool) was adapted for photonic simulations and was used in eigensolver configuration to calculate the mirror strength of the cavity unit cells at a resonance wavelength of 1520 nm as a function of a taper parameter. Once the cavity design was synthesized, HFSS was also used to find the fundamental and higher order modes of the full cavity and to analyze the effects of

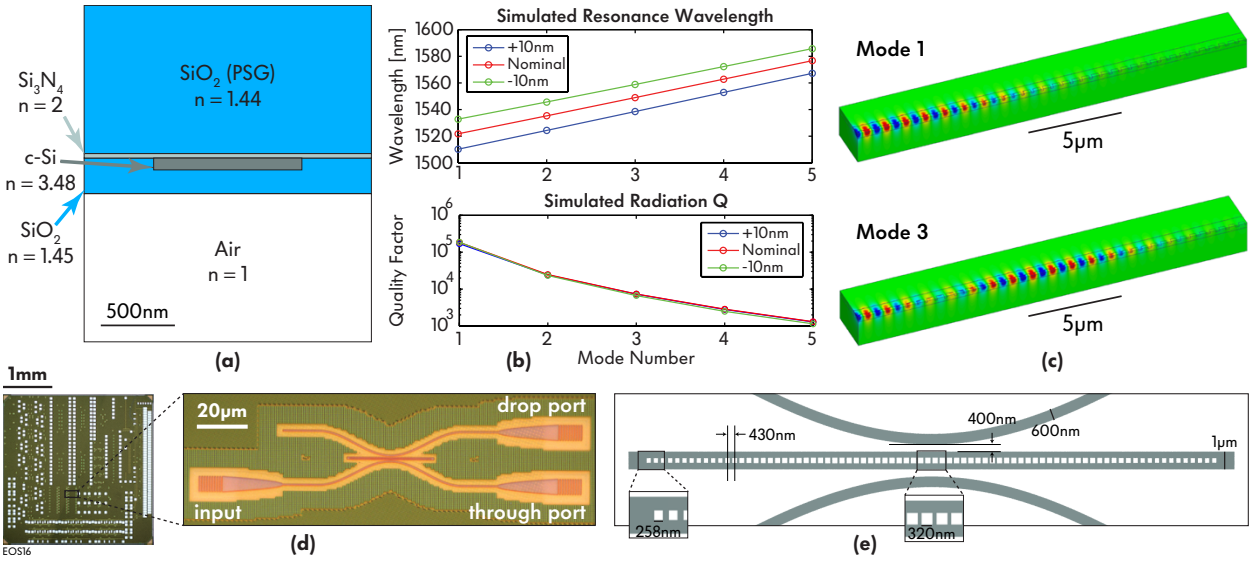

Fig. 1. (a) Partial cross-section representative of IBM 45 nm 12SOI CMOS process (details in PDK [11]). (b) 3D HFSS simulated resonances and radiation Q's for first few resonant modes. (c) Transverse electric field distribution of first and third mode of the cavity from HFSS. (d) Optical micrograph of a fabricated device. (e) Cavity device layer layout.

fabrication variations. Fig. 1(b) shows the resonance frequencies and radiation Q's simulated for the synthesized cavity as well as for ones with ± 10 nm variations in dimension of the square holes. The fundamental mode has a simulated intrinsic quality factor of 184k at 1521 nm. The intrinsic Q decreases exponentially with mode number. This is because the cavity length is fixed, and holes stop after a total of 80 periods. This discontinuity in the parabolic potential allows the more delocalized higher order modes to tunnel out to the silicon guide. Fig. 1(c) shows the field profiles of the first and third mode of the synthesized cavity.

The cavity is excited via evanescent coupling from two side-coupled waveguides, an input and a drop waveguide, in a symmetric configuration. In comparison to direct excitation from the waveguide in which the cavity is formed, such a coupling geometry has the advantage that the cavity design is completely independent of coupling design; the cavity-waveguide gap is the only parameter changed. In this configuration, the ideal transmission on resonance is -6 dB (25%) to all four ports due to the symmetry of the standing-wave cavity system [8]. Fig. 1(d) shows an optical micrograph of a fabricated device, and Fig. 1(e) shows the device dimensions.

3. Experimental Results

Fig. 2(a) shows measured through port responses of three cavities – the nominal design and the ± 10 nm hole variants. All cavities show a number of resonances in the measured 80 nm window, as expected due to the extended cavity length. The nominal design shows a fairly constant FSR near 1.52 THz (1.71 THz in design). In all three designs, the measured fundamental mode resonance wavelength is 7 nm lower than design. The resonance and FSR shifts can be explained by a silicon device layer thickness variation within the process tolerances and lithographic proximity effects on the hole tapering.

Figs. 2(b,c) show the through and drop port spectra of the -10 nm cavity design and a close-up view of the fundamental mode which shows transmission near the ideal value of -6 dB, i.e. operates as a wavelength selective 4-way power splitter. The bandwidth is 92 GHz (a total Q of 2,150). A simple coupled-mode theory model [8] may be used to extract the external Q due to loading waveguides and intrinsic loss Q of the cavity, to evaluate the cavity performance. For a device with this geometrical symmetry, all that is needed is the on-resonance transmission and bandwidth of the through port response. Fig. 2(d) shows the disembedded loss and external Q's of the -10 nm design cavity for the first three modes, showing an external Q of 2,190 (total, to both waveguides) and a loss Q of $\sim$100,000 for the first mode.

We noted that the loss Q exponentially drops with mode number and explained this as a tunneling to the guided nanobeam waveguide mode at the edges of the cavity. This was confirmed by IR images of the $+10$ nm design device [Fig. 2(e)] when each of the first three modes was excited on resonance. In all three cases, scattering is seen at the terminated waveguide port as well as the through and drop port grating couplers, as expected for a standing wave cavity that radiates to all four ports. The cavity is dark on resonance which is a good indicator that radiation loss at least within the NA of the microscope objective is small and is consistent with high Q. On the two higher order modes,

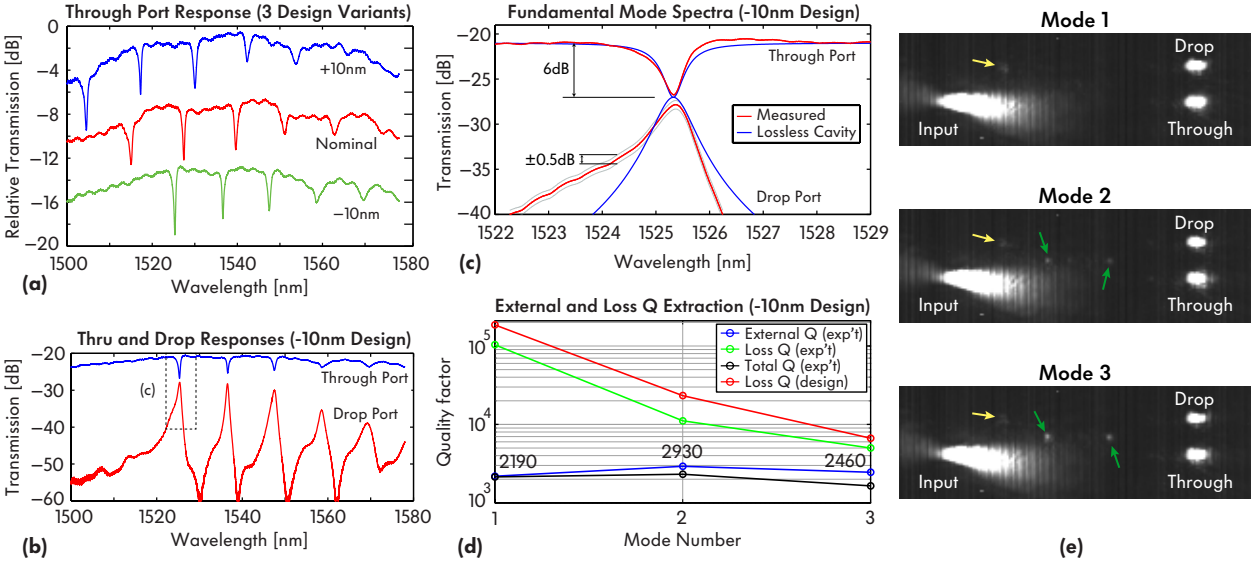

Fig. 2. (a) Cavity through port responses. (b) Through and drop port response of the −10 nm design cavity, and (c) its fundamental mode along with an ideal response. (d) Measured total, external and loss Q's, and design loss Q of the first three modes for the −10 nm design cavity. (e) Top view IR images of +10 nm design cavity on resonance. Arrows point to scattering at shunt waveguide (yellow), and scattering on the edges of the cavity nanobeam (green).

some scattering is seen also on the edges of the cavity itself. This is consistent with the increased tunneling radiation loss for the higher order modes as predicted.

That the device has near the ideal −6 dB transmission indicates that most power is coupled to ports and that the loaded Q is much lower than the intrinsic Q. Therefore, parameter extraction to find the loss Q of the cavity is sensitive to errors – a better than 5.3 dB extinction ensures a loss Q of >25,000, and an extinction better than 5.84 dB ensures a Q >100,000. Measured spectra give extinction of 5.94 dB when normalizing out the grating coupler response. We estimate an uncertainty of about 0.1 dB due to Fabry-Perot oscillations, so the cavity loss Q (including radiation, scattering and coupling induced loss) is on the order of 100k.

Another observation in this coupling geometry is that the extracted external (waveguide coupling) Q is higher for the second mode than for the first, but then lower again for the third mode while still higher than the first [Fig. 2(d)]. This is consistent with expected behavior. Higher order modes should have weaker coupling and higher Q, because the modes are larger in volume, while the power coupled to the waveguide (from the center of the cavity) is similar. A modification for even-numbered modes is that they have a field null in the center of the cavity where the coupler is located. This means that they have a suppressed coupling to the bus waveguide and a higher external Q.

The demonstrated linear photonic crystal cavities integrated within an advanced SOI CMOS process show respectable quality factors and will enable new possibilities for efficient devices in monolithic CMOS photonics. This work was supported by DARPA POEM program award HR0011-11-C-0100, and by the University of Colorado Discovery Learning Apprenticeship (DLA) undergraduate program.

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