A Monolithically-Integrated Chip-to-Chip Optical Link in Bulk CMOS

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Abstract—Silicon-photonics is an emerging technology that can overcome the tradeoffs faced by traditional electrical I/O. Due to ballooning development costs for advanced CMOS nodes, however, widespread adoption necessitates seamless photonics integration into mainstream processes, with as few process changes as possible. In this work, we demonstrate a silicon-photic link with optical devices and electronics integrated on the same chip in a 0.18 μm bulk CMOS memory periphery process. To enable waveguides and optics in process-native polysilicon, we introduce deep-trench isolation, placed underneath to prevent optical mode leakage into the bulk silicon substrate, and implant-amorphization to reduce polysilicon loss. A resonant defect-trap photodetector using polysilicon eliminates need for germanium integration and completes the fully polysilicon-based photonics platform. Transceiver circuits take advantage of photonic device integration, achieving 350 Gb/s transmit and 71 μA receiver sensitivity at 5 Gb/s. We show high fabrication uniformity and high-Q resonators, enabling dense wavelength-division multiplexing with 9-wavelength 45 Gb/s transmit/receive data-rates per waveguide/fiber. To combat perturbations to variation- and thermally-sensitive resonant devices, we demonstrate an on-chip thermal tuning feedback loop that locks the resonance to the laser wavelength. A 5 m optical chip-to-chip link achieves 5 Gb/s while consuming 3 pJ/b and 12 pJ/bit of circuit and optical energy, respectively.

Index Terms—Memory, optical interconnects, optoelectronics, process integration, silicon-photonics, wireline transceivers.

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complexity and packaging yield concerns, ultimately raising even more barriers to widespread photonics adoption.

To gain traction among high-volume applications, such as memory, electronic-photonic integration must be demonstrated monolithically in bulk silicon. Compared to SOI, a bulk platform faces two additional challenges. The first is the lack of a thin crystalline silicon layer present natively on the wafer, necessitating polysilicon-based waveguides [17], [18], which can be much more lossy due to crystal grain imperfections. Alternatively, crystalline silicon may be epitaxially grown as the waveguide material [7], but the high temperature processing has thus far proved to be a risk to process-native transistors. The second challenge is the lack of a thick BOX layer for waveguide isolation from the substrate. The undercut technique [17] requires post-processing and constrains circuit-photonics placement. The extension of shallow-trench isolation to make deep oxide-filled trenches underneath optical waveguides [7], [18] is an alternative that enables tighter integration without post-processing, but requires additional process integration. Because of these challenges, electro-optic transceivers and links in monolithic bulk processes have yet to be demonstrated.

This paper introduces a monolithically-integrated bulk photonic platform and presents the devices and circuits that form the componentsof a DWDM link, culminating in a chip-to-chip link that demonstrates the feasibility of this platform. We take an existing bulk process and enable photonics in the most CMOS-friendly way possible—all in polysilicon—while identifying the best DWDM-suitable devices and circuits that can be built effectively under these constraints.

The rest of the paper is as follows. Section II provides an overview of optical microring resonator devices—a fundamental building block for DWDM—that demonstrates the feasibility of this platform. We take an existing bulk process and enable photonics in the most CMOS-friendly way possible—all in polysilicon—while identifying the best DWDM-suitable devices and circuits that can be built effectively under these constraints.

The key building block of a DWDM link is the optical microring resonator (Fig. 2). When coupled to a waveguide, the ring captures only light at its resonant wavelength, forming a notch filter. A wavelength is resonant when the ring circumference is an integer multiple of λ. Resonances are periodic with a spacing defined as the free spectral range (FSR), which grows with a smaller circumference. Due to this periodicity, all λ used in a DWDM link must fit within one FSR, where each ring has single-λ selectivity. The quality factor of the microring resonator is dictated by the full-width half-maximum (FWHM) bandwidth of the notch and the intrinsic extinction ratio is defined as the depth of the notch. Doping and contacting the ring in active structures (modulators or photodetectors) lowers the quality factor by introducing loss from free carrier absorption. is primarily a factor of the coupling between the ring and the bus waveguide, tuned by the gap between them. A ring that is perfectly critically coupled (defined as when the power coupled from the bus waveguide matches the energy decay rate due to losses in the microring) provides infinite Q. When not that a higher Q-factor yields a greater modulation depth given the same change in but also translates to a higher lifetime for photons resonating in the ring. Photon lifetimes comparable to or greater than the bit time result in optical ISI due to residual light left in the ring from bit-to-bit.

An electro-optic microring modulator can be realized by modulating the resonance (λ₀) to perform on-off-keying...
Fig. 2. The optical transfer characteristics of a microring resonator (a waveguide looped around in a ring to form a resonating cavity) that is resonant at $\lambda_0$.

Fig. 3. Ring resonators used in a modulator and a receiver. The input light is at the same wavelength as $\lambda_0$. The modulation insertion loss (IL) and the extinction ratio (ER) are defined as $10 \cdot \log_{10} T_1$ and $10 \cdot \log_{10} T_1/T_0$, respectively. $T_1$ and $T_0$ represent modulated output powers for optical ones and zeros, normalized to the input power.

(OOK) of input light aligned close to $\lambda_0$ (Fig. 3, left). Changes in free carrier concentration are used to shift $\lambda_0$ by changing the material's index of refraction [21]. Carrier-injection modulators are p-i-n junctions that inject carriers into the intrinsic region during forward-bias, blue-shifting $\lambda_0$. Carrier-depletion modulators are p-n junctions that deplete the carriers from the junction during reverse bias, red-shifting $\lambda_0$. Carrier-injection modulators are limited in speed by minority carrier lifetimes, necessitating pre-emphasis schemes to reach higher data-rates [9], [15], [22]. Forward-biased operation of the junction also results in static power dissipation and poor energy-efficiency. Carrier-depletion designs avoid these issues, but require better doping control to balance $\lambda_0$ shift with Q-factor degradation from free carrier absorption. Rings also perform receiver channel wavelength selection, dropping only light at $\lambda_0$ onto a photodetector (PD), which is broadband (Fig. 3, right). Embedding the PD in the ring itself [23] can enhance optical absorption for a given PD size. However, integration of the PD material (typically Germanium) into the ring can be challenging.

An increase or decrease in temperature causes a resonance red-shift or blue-shift (through a change in index of refraction), respectively, of roughly 10 GHz/K (55 pm/K at 1280 nm). The strong thermal dependence enables integrated microring heaters to combat resonance variations from limited process tolerances [19], [24], but also necessitates active resonance control when microrings are integrated in an electrical system, where temperatures fluctuate. Because thermal variations are slow, however, wavelength-locking can be achieved with low overheads [9], [25]–[28].

III. MONOLITHIC PHOTONICS PLATFORM IN BULK

The monolithic bulk platform is demonstrated in a 0.18 $\mu$m 3-metal-layer bulk CMOS process. We construct all optical devices in polysilicon, including the photodetector. Electronics are built from the power-optimized NOR flash periphery transistors native to the process, with FO4 delays of approximately 80 ps and 65 ps with 2 V and 2.5 V supplies, respectively. In contrast to standard logic processes, the platform represents a low-cost high-volume application, such as memory, where transistors are slower.

To enable photonics, we make three key modifications to the original CMOS process [29], shown in Fig. 4. The first is the addition of a silicon implant amorphization step for the polysilicon used in optical devices. This lowers the loss of waveguides built using process-native gate polysilicon from 40 dB/cm to 18 dB/cm [18]. Further nitride spacer optimizations bring the loss down to 10.5 dB/cm at process end-of-line [29]. The losses compare favorably to the 2 dB/mm (20 dB/cm) losses reported in [7] for waveguides built using expitaxially grown crystalline silicon in an electronic-photonic process flow. The second is the inclusion of a deep-trench isolation step (DTI) to avoid post-process undercut. DTI creates a 1.2 $\mu$m oxide-filled trench underneath polysilicon waveguides to provide optical waveguide mode confinement and isolation from
Fig. 4. Photonics platform cross-section. The step-like shape of the polysilicon ridge waveguide and vertical coupler grating teeth are enabled via the partial polysilicon etch.

Fig. 5. Structure of the carrier-depletion ridge waveguide modulator used in the transmitter (a) and its measured thru-port transfer characteristics under different applied DC voltages (b). We estimate a modulator junction capacitance of 20 fF and a series resistance of 500 Ω, corresponding to a 15.9 GHz device RC bandwidth.

The optical modulator device is a carrier-depletion microring modulator constructed using a polysilicon ridge waveguide (enabled by PPE) and doped with mid-level implants as a p-n junction (Fig. 5). The ridge structure confines the optical mode to the center of the ridge, allowing electrical contacts on the sides to avoid overlap with the optical mode. The modulator ring has a radius of 7.25 μm with an FSR of 1.6 THz (9 nm). We pick this radius conservatively to make radiative tight-bend losses negligible; rings with 3 μm radii and an FSR of 3.7 THz have been demonstrated previously in the same platform [31].

Measured optical transfer characteristics of this device under different DC voltages (Fig. 5(b)) shows a resonance shift of 2.7 GHz/V (15 pm/V) and that weak forward-biases can be applied to increase the total shift. The ring has a Q-factor of 8000 (28.8 GHz FWHM) and an ER, of 15 dB. Note the higher ER, under reverse bias and the lower ER, in forward-bias. This is indicative of slight undercoupling, as the depletion of carriers (which lowers the free-carrier loss) moves the ring closer to critical coupling.

To avoid the introduction of germanium—found in all custom photonics platforms to date [7], [8], [13], [32]—we employ a completely polysilicon-based photodetector utilizing absorption from defect states [33]. This photodetector is a ridge-waveguide microring (with matching radius and FSR as the modulator device) doped with a p-i-n junction (Fig. 6(a)). When light resonates in the ring, sub-bandgap photoabsorption stemming from defect states in the polysilicon generates free-carriers. Though this absorption is nominally weak, the resonant structure significantly enhances the effective absorption length, achieving a PD responsivity of 0.2 A/W in both the 1280 nm and 1550 nm wavelength bands. The device exhibits 3 dB photoresponse bandwidths of 1.5 GHz and 7.9 GHz at −1 V and −10 V biases, respectively. Due to much lower end-of-line waveguide losses than expected during design time, all receive macros with the best-performing receiver circuit connect to PD-microrings that are severely overcoupled (Fig. 6(b)). These exhibit a Q-factor of only 4000 (60 GHz FWHM) and an ER, of 2.4 dB. This can be fixed in the layout by increasing the ring-to-waveguide gap to weaken the cou-
Fig. 6. Structure of the resonant polysilicon defect photodetector used in the receiver (a) and its measured thru-port transfer characteristics (b). We show the case for both a critically-coupled ring and the severely overcoupled ring (which is the version connected to the receiver circuits). Note the linear scale in the transfer characteristic. The photodetector capacitance is estimated to be 15 fF.

Fig. 7. Monolithically-integrated photonics platform in bulk. Shown here is an example of a single-λ chip-to-chip optical link using a transmit macro from chip 1 and a receive macro from chip 2.

pling and the gap can be set appropriately at design time once the waveguide loss is known. Critically-coupled, but otherwise identical, PD rings appearing elsewhere on the chip achieve a quality factor of more than 9000 (26 GHz FWHM) and an ER of 25 dB.

We build the optical link components as part of a 24 mm×24 mm technology development reticle for testing a variety of optical devices and circuits. The reticle is divided into standalone optical device regions and an array of ten 5 mm×5 mm transceiver chiplets, which are individually wirebonded and packaged electrically. Each chiplet hosts an array of 8 single-λ electro-optic transceiver macros (Fig. 7) and three 9-λ DWDM transceiver macros for a total of 5.5 million transistors and 100 optical devices per chiplet.

Each single-λ macro consists of a synthesized digital backend and custom high-speed transmit and receive heads that connect to the optical devices. The backend runs at one-fourth the data clock and interfaces with the custom heads through 8-to-2/2-to-8 CMOS mux/demux tree SerDes. PRBS31 generators and bit-error-rate (BER) checkers in the backend perform in situ characterization of the transceivers. Heater driver and tuning components drive integrated ring heaters and contain programmable logic for closed-loop wavelength-locking. Optical waveguides, couplers, and active devices are instantiated in
rows alongside the circuits. Single-mode fibers (with a cleaved tip) are positioned over the VGCs (using probe positioners or mounted to the package) to couple light in or out of on-chip waveguides. The 9-λ DWDM transceiver macros are similar to nine adjacent single-λ macros, but string together all nine modulator- or receive-microrings on a single bus waveguide to provide DWDM functionality.

IV. DEPLETION-MODE MICRORING OPTICAL TRANSMITTER

The transmitter consists of a depletion-ridge modulator device driven by a transmitter frontend circuit, shown in Fig. 8. The frontend circuit consists of a 2-to-1 DDR serializer followed by an inverter-based push-pull driver. The NMOS pull-up transistor in the final driver stage on the anode terminal is used to limit the applied forward-bias voltage. On logic 1 s, the transmitter circuit applies a voltage of $V_{\text{REF}} - V_{\text{T}}$ to the modulator junction, depleting the junction of carriers and red-shifting the resonance. On logic 0 s, the circuit weakly forward-biases the device to a voltage of $V_{\text{REF}} - V_{\text{T}}$ to inject carriers into the junction and blue-shift the resonance.

The choice of where to bias the laser wavelength relative to the resonance is a degree of freedom for a ring modulator. We define an eye-height metric, $\Delta T$, as the difference in optical powers for modulated logic 1 and logic 0 levels, normalized by modulator input optical power:

$$\Delta T = T_1 - T_0 = |10^{-IL/10} - 10^{-(IL+ER)/10}|$$

where $IL$ is the modulator insertion loss and $ER$ is the modulator extinction ratio, both given in dB. Using this metric, we perform an optimization to find the maximum eye-height that this device can support, shown in Fig. 9. Note that the optimal eye-height is not located at the same wavelength as the one that gives the greatest $ER$; though $T_0$ is suppressed far below $T_1$ at this point, the noticeable higher $IL$ degrades the level of $T_1$. Conversely, bias points far away from the resonance have low $IL$ but provides too little $ER$ to create sufficient modulation depth. The optimum occurs at a point where $IL$ and $ER$ are balanced against each other, e.g., $IL = 2.0$ dB and $ER = 6.6$ dB for the shown modulator, corresponding to $\Delta T = 0.49$.

We measure the modulator under two sets of modulator operating voltages, case 1 and case 2, achieving open-eye data-rates of 4 Gb/s and 5 Gb/s, respectively, with a PRBS31 sequence (Fig. 10). The maximum data-rate of the transmitter is limited by transistor performance; At 5 Gb/s, the higher voltage in case 2 is necessary to maintain correct digital functionality in the 2-to-1 serializer and sufficient overdrive on the pull-up NMOS transistor for a fast edge. Photon lifetime effects from the microring linewidth itself ($Q = 8000$, 28.8 GHz optical bandwidth) are negligible at these data-rates. Note that the experimentally measured $ER$ and $IL$ are better than what is expected from the DC wavelength scans. This is because under sufficiently large forward bias (blue-shift), self-heating from diode on-current acts to red-shift the ring slightly back, making the shift captured by the DC measurement appear smaller. As data-transmission is at a much higher rate than the thermal time constant, the modulated eye captures the true extinction of the device. The measured energy-per-bit of the modulator across data-rates is shown in Fig. 11. The clock buffers driving the serializer dominate total power due to aggressive sizing for 3x FO4 target bit-times and phase-matching of the inverted phase for the 2-to-1 CMOS DDR multiplexer. At the $V_{\text{REF}}$ used in case 2, the driver applies a sufficiently large forward-bias voltage to weakly carrier-inject the modulator diode, drawing additional static current on logical 1s. The static current is amortized at higher data-rates, hence the small efficiency improvement with data-rate. Case 1 pushes the device into weak carrier-injection to a smaller extent due to lower $V_{\text{REF}}$. The driver energy efficiency is 200 fJ/bit at 4 Gb/s and 350 fJ/bit at 5 Gb/s for case 1 and case 2, respectively, with an overall energy-efficiency of 0.7 pJ/b and 1.16 pJ/b for the full transmit circuit, which includes the clock.
buffers and 2-to-1 serializer. For the macro floorplan to be compatible across all types of optical devices on the platform, we had to place the modulator device 60 μm away from the frontend circuit, adding wiring capacitances of 13 fF and 14 fF (from layout extraction) on the anode and cathode nodes, respectively. We estimate that an optimized device-to-circuit placement using the minimum 2 μm spacing will reduce wiring capacitances down to sub-2 fF, extending the achievable data-rate and lowering the energy cost further.

We build the transmitter circuit as part of a 9-λ DWDM transmit macro, shown in Fig. 13. The rings are spread across the 9 nm FSR and we step the radii to achieve a nominal 1 nm channel-to-channel spacing (Fig. 12), achieving more than 20 dB of cross-talk isolation between adjacent channels. Across the 3.5 mm span of the rings, no ring experiences more than 0.5 nm deviation from its nominal resonance and local variations are not large enough to flip the ordering of adjacent channels on any measured chip or wafer. We use the tuning circuits in the backend to drive integrated microring heaters to move rings back to the grid. We verify that the macro is capable of an aggregate 45 Gb/s of data transmission through a single waveguide or fiber by individually capturing an open transmit

Fig. 10. Transmitter characterization setup. The eye-diagrams are shown for case 1 at 4 Gb/s and case 2 at 5 Gb/s.

Fig. 11. Measured transmitter energy-per-bit. The component-level power breakdowns are deembedded through simulation using extracted netlists that include the wiring capacitances on the modulator anode and cathode (extracted to be 13 fF and 14 fF, respectively) and a 20 fF modulator junction capacitance.

Fig. 12. Optical thru-port transfer characteristic of the 9-λ DWDM transmit bank. The tuned spectra is after coarse tuning to a 1 nm grid. Each resonance is numbered with its corresponding ring.

eye on each of the 9-λ slices at 5 Gb/s (Fig. 13). The I/O density of the DWDM macro is approximately 110 Gb/s/mm², including all transmitter circuits (120 μm x 50 μm per slice) and a conservative (3500 μm x 100 μm) trench for the photonic devices. Note that the ring-to-ring placement pitch of 384 μm
V. POLYSILICON-BASED RESONANT OPTICAL RECEIVER

The receiver block is composed of a ring resonant defect-detector connected to a receiver circuit, shown in Fig. 14. To mitigate the slow speed of the process, we adopt a split-diode technique [23]; each PD microring is separated into two electrically-isolated PD-halves (PD-0, PD-1), each connected to a receiver-half (RX-0/1) running at half-rate on opposite clock phases. In effect, each receiver-half gets $1/2$ of the total photocurrent ($I_{PD}$), but is given twice the evaluation time. Each receiver-half circuit consists of an inverter-based TIA followed by a clocked sense-amplifier and RS latch. The TIA transimpedance gain can be adjusted by configuring the feedback resistor to be $12 \, \text{k}\Omega$ or $4 \, \text{k}\Omega$. Current and capacitive DACs attached to the sense amplifier provide offset compensation and eye-measurement capability for the receiver.

We design the circuit to accommodate a potentially large dark current range across all PD variants on the platform reticle; the dummy PDs and TIAs serve as dark current references, keeping the sense-amps balanced for large dark currents. Under extremely high dark currents, the current DAC at the input of each TIA cancels dark currents to keep the TIA biased in a linear regime. We note, however, that there is less than $50 \, \text{pA}$ of dark current at a $-10 \, \text{V}$ bias for the defect microring PD [33]. Hence, the dark currents are low enough for the dark current cancellation DAC and dummies to be removed in a receiver tailored specifically for this device.

A sense-amp undergoes two phases during evaluation time: a linear integration phase in which $v_{in}$ is integrated onto the cap through the $g_m$ of the input transistor and an exponential regeneration phase where the positive feedback of the cross-coupled inverters drives $v_{out}$ to the supply rails. The behavior of the sense-amp can be modeled, to first-order, as:

$$v_{out} = v_{in} \frac{g_m}{C_{in}} \cdot t_{int} \cdot e^{\frac{-t_{regen}}{t_{inv}}}$$  \hspace{1cm} (2)
where \( t_{\text{int}} + t_{\text{regen}} = t_{\text{eval}} \). The onset of regeneration (and the end \( t_{\text{int}} \)) is triggered when the voltage at the drain of the input transistor drops sufficiently low to trigger a loop-gain > 1 in the cross-coupled inverters. In traditional sense-amps, this is set by the sizing of the footer and the common mode of the input transistor and does not change automatically when \( t_{\text{real}} \) shrinks with data-rate. Accordingly, a shorter evaluation time will directly squeeze \( t_{\text{regen}} \), degrading the sense-amp sensitivity exponentially once \( t_{\text{regen}} \) is no longer sufficient to regenerate rail-to-rail. Like-wise, a \( t_{\text{int}} \) that is too short results in a \( t_{\text{regen}} \) that is more than sufficient to fully regenerate rail-to-rail, wasting time that could have been used to integrate a larger input. To minimize sense-amp sensitivity \( v_{\text{in}} \), the \( t_{\text{int}} \) should be traded off with \( t_{\text{regen}} \) to balance linear growth with exponential growth. We perform this optimization in the receiver by switching on both sides of the current compensation DAC simultaneously. We size the receiver for relatively long \( t_{\text{int}} \) for better sensitivity at low data-rates and switch on the current DACs to reduce \( t_{\text{int}} \) and boost \( t_{\text{regen}} \) for higher rates as \( t_{\text{eval}} \) shrinks. This comes at a small cost in static power, but allows for an optimal split between \( t_{\text{int}} \) and \( t_{\text{regen}} \) across a wide data-rate range.

We measure the receiver in a high-performance mode (\( V_{\text{DD}} = 2.5 \) V) and a low-power mode (\( V_{\text{DD}} = 2.0 \) V), biasing the PD at \( V_{\text{PD}} = -10 \) V for all experiments (Fig. 15). The receiver runs with no bit-errors up to 5 Gb/s and 3 Gb/s for \( 2 \times 10^{12} \) bits (\( 10^{12} \) bits on each receiver-half) in the high-performance and low-power modes, respectively. Beyond 5 Gb/s, the sense-amp is too slow to maintain correct functionality. The high-performance mode achieves a \( 10^{-12} \) BER sensitivity of 12 \( \mu A_{\text{pp}} \) (-15.2 dBm with a 0.2 A/W PD) for 1 Gb/s–3 Gb/s. At 5 Gb/s, sensitivity degrades to 126 \( \mu A_{\text{pp}} \) and 71 \( \mu A_{\text{pp}} \) (-7.5 dBm) before and after the sense-amp \( t_{\text{int}} \) optimization, respectively. The low-power mode achieves comparable sensitivity at half the power up to 3 Gb/s, when the \( t_{\text{eval}} \)-limited sense-amp begins degrading sensitivity.

A layout error resulted in the placement location of the dummy PD microring and the active PD microring to be swapped, causing the active PD to be placed 150 \( \mu m \) farther from the receiver than the dummy PD. From layout extraction,
This error lowers the TIA bandwidth by approximately 1/3, causing the 12 kΩ feedback resistor to have insufficient bandwidth to support data-rates beyond 3 Gb/s. The reduction of the TIA feedback resistance to 4 kΩ, coupled with the smaller sense-amp $t_{\text{eval}}$, results in the degradation of sensitivity past 3 Gb/s. Power consumption of the full receiver is dominated by the static TIA power, which is amortized at higher rates. Elimination of the dummy dark-current matching TIAs in future designs will halve the TIA power component. The receive macro follows the same floorplan as that of the transmit macro and can likewise be optimized to move devices closer to circuits to lower wiring capacitances.

We verify receivers integrated into a 9-λ DWDM receiver macro by individually aligning the laser to each λ-slice and measuring the BER (Fig. 16). We record error-free receiver eye openings for $2 \times 10^{10}$ bits on each slice at 5 Gb/s, demonstrating that the macro is capable of 45 Gb/s aggregate receive bandwidth per waveguide or fiber (114 Gb/s/mm²). Fig. 17 shows the macro’s optical spectrum. The macro is FSR-matched to the DWDM transmit macro with the same channel spacing (1 nm). PDs in the tested DWDM macro are also severely overcoupled with $ER_i < 3$ dB ($Q = 4000$, 15 dB crosstalk isolation at 1 nm spacing). A separate DWDM receiver macro with critically-coupled PD rings exists elsewhere on the same chip ($Q = 9000$, 23 dB crosstalk isolation at 1 nm spacing), though it is connected to a different kind of receiver.

VI. RING RESONATOR WAVELENGTH LOCKING

In this section, we demonstrate an on-chip wavelength-locking circuit that maintains the receiver eye opening under changing temperatures. The synthesized receive-side tuning sub-system (Fig. 18) contains an optical power meter circuit, a configurable data path, a programmable lookup-table (LUT), and a $\Delta \Sigma$-DAC circuit [31] that drives an integrated microring heater. As opposed to tracking an averaged photocurrent [9], [25], [26], [28], which can mistake changes in the 1/0-balance of the data (which is on-off encoded) for a drift in resonance, the power meters are conditioned on the received data to track the one or zero levels directly. Level-trackers were previously proposed in [27], [34], and [35] to actively adjust receiver threshold levels given variances in signal power. Here, we use the tracked photocurrent-level as an indication for how the ring’s resonance has drifted in order to move the resonance back to its desired position. Due to area constraints in the platform, we reuse the receiver-half circuit in a bang-bang loop to act as a 5 bit sense-amp based ADC (with the capacitative offset compensation DACs serving as the voltage DAC) in the power meter. During wavelength-locked receiver operation, the power meter takes control of one receiver-half and uses the data stream from the other half, which receives data normally, to use as the conditioning signal. The controller consists of several registers and LUTs that provide flexibility in programming a variety of control schemes, based on current and
previous power meter outputs and arbitrary threshold values. The output of the controller is an 8-bit binary value for the heater strength. A ΔΣ-DAC (described in [31]) drives the integrated heater. All tuning backend circuits are clocked by the data-clock through a divide-by-64 divider.

The lock range of the tuner is 0.5 nm (90 GHz) [36], corresponding to a 9 K change in temperature. In the context of the 9-λ transmit and receive DWDM macros, this range is marginally sufficient to tune out local process mismatch but is still less than the total desired (1.5 nm); applying the ring-to-λ assignment shifting schemes from [19], the tuning range needs to be around that of the channel spacing (1 nm) plus the worst-case local process variation (0.5 nm) to guarantee that each ring can be assigned and tuned to a laser channel λ across all temperatures. Currently, the tuning range is limited by the maximum heater output power of 6 mW (limited by the 1 kΩ resistance of the integrated heater and the 2.5 V supply). The tuning range will increase by using a lower heater resistance or by improving the tuning efficiency, which we estimate to be 67 μW/GHz (108 mW/FSR). As a comparison point, a 3 μm radius ring on the same platform with optimized heater placement demonstrated a tuning efficiency of 10 μm/GHz [31].

We perform a 2.5 Gb/s single-rate transient wavelength-lock experiment, shown in Fig. 19. We clock-gate on/off the various components in the digital backend of adjacent transceiver macros to create a temperature aggressor. These induce a microring temperature change of approximately 20 K for every Watt of power they dissipate. In this experiment, we program the controller with a simple tuning scheme where we simply heat more if the power meter reading exceeds a set threshold and heat less if the readings are less. The wavelength-locked receiver is completely error-free until 65 seconds into the test, when we apply a deliberately large temperature change (approximately 11 K) to exceed the lock range to force failure. By contrast, an unlocked receiver fails immediately with any temperature perturbations caused by the aggressor due to a drop in photocurrent caused by the drift in the ring’s resonance. The tuning backend consumes 0.43 mW at 2.5 Gb/s (171 fJ/bit) and 0.024 mm², excluding the heater driver and the receiver. The area is largely dominated by the LUT and data-path and the tuning algorithm can also be synthesized directly into gates at design time to conserve power and area.
VII. MONOLITHIC CHIP-TO-CHIP LINK IN BULK

Using the transceiver macros, we build a chip-to-chip optical link through 5 m of single-mode fiber interconnecting the two chips (Fig. 20). We note that this demonstration uses a single $\lambda$ and clocks are forwarded to both chips electrically. Normally, in a DWDM configuration with multiple $\lambda$s, the clock would be available as a transmit-forwarded signal on one of the other chips.
wavelengths. We demonstrate a full-rate 2 Gb/s chip-to-chip link that is error-free for $2 \times 10^{12}$ bits. The maximum data-rate of the link is currently limited by the degradation of receiver sensitivity at higher rates and the 10 mW maximum output power of the off-chip laser. We currently hit this limit due to an extra 9 dB of optical loss caused by a sub-optimal permutation of optical devices in the transceiver macros; VGCs in the transceiver macros contribute 5 dB of loss per coupler, compared to the 3 dB loss VGCs present elsewhere on the platform. Additionally, the severely overcoupled photodetector rings (2.4 dB ER$_s$) effectively results in another loss of 3.7 dB. To overcome the loss with the current combination of devices, we insert an optical amplifier between the transmit chip and the receive chip, which adds approximately 8 dB of optical gain and enables 5 Gb/s operation for the link. The link consumes 4 pJ/b electrical and 5 pJ/b optical energy at 2 Gb/s. At 5 Gb/s, the link consumes 3 pJ/b electrical and 12 pJ/b optical energy.

We perform a link power analysis across a range of data-rates using the metrics from the measured circuits (Fig. 21). We calculate the wall-plug laser power of the link as

$$P_L = \frac{1}{\eta_e} \cdot \frac{S_i}{R_{pd}} \cdot \frac{1}{1 - 16 \cdot E/R/10} \cdot 10^{L/10}$$

where $\eta_e$ is the laser wall-plug efficiency, $S_i$ is the receiver sensitivity (in $A_{pp}$), $R_{pd}$ is the photodetector responsivity, $E/R$ is the modulator extinction ratio and $\sum L$ is the total optical loss in the path from the laser to receiver. For this analysis, we assume an $\eta_e = 25\%$. We show a case using devices currently in the transceiver macros and a case using best-known devices on the current platform. In both cases, the link is most energy-efficient at a data-rate of 3 Gb/s–4 Gb/s. Static power (microring heating/tuning, receiver TIA, the receiver) is amortized at higher rates. Energy-per-bit from the laser also decreases initially from 1 Gb/s–3 Gb/s, where $S_i$ (and hence $P_L$) remains flat. At the higher rates, $S_i$ increases drastically and offsets the energy-per-bit improvement from the higher data-rate. For the case using the current set of devices in the transceiver macros, the laser wallplug power dominates the energy-per-bit, reaching an optimal wallplug link energy of 18.3 pJ/b at 3 Gb/s. In the second case, the better devices reduce optical loss by more than 9 dB. As such, the laser is no longer dominant for 1 Gb/s–4 Gb/s and an optimal energy efficiency of 6.5 pJ/b is reached at 4 Gb/s.

**VIII. CONCLUSION**

To facilitate the adoption of photonics for mainstream CMOS applications, we must first remove its intimidation factor: prove that the technology is viable for electronics integration without exotic processing steps, customized SOI wafers, or complicated packaging. To this end, we demonstrate a polysilicon-only monolithic photonics platform in bulk CMOS, to show that low-loss waveguides and active optical structures can be integrated through a minimal number of process changes. By avoiding epitaxially grown crystalline silicon for waveguides and finding an alternative to germanium integration for photodetectors, the polysilicon-only photonics module minimizes risks to process-native transistors and improves technology portability.

We build a portfolio of DWDM link components—a DWDM transmitter and a DWDM receiver—each demonstrating competitive performance and efficiency despite the early stage of platform development. We further improve the robustness of the wavelength-locking techniques by resolving the data-dependency challenge, demonstrating that robust DWDM ring tuning is feasible in a hostile temperature environment. We compose an optical chip-to-link, which, to the knowledge of the authors, is the first demonstration of a monolithically-integrated optical link in a bulk CMOS process. The unique polysilicon aspects of this photonic platform make it independent of the front-end integration processes, enabling deployment in more advanced
bulk CMOS process nodes to further scale the link performance and energy efficiency.

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References


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