Microphotonic Channel Add-Drop Filter Based on Dual Photonic Crystal Cavity System in Push-Pull Mode

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Abstract: We demonstrate an add-drop filter based on a dual photonic crystal microcavity system that emulates a traveling-wave resonator. Realized on a 45 nm SOI CMOS chip, the device shows 16 dB through-port extinction and 1 dB drop loss.

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In wavelength division multiplexing (WDM) schemes, channel add/drop optical filters are a critical component and have been previously demonstrated using microring resonators [1] whose traveling-wave (two-degenerate mode) structure enables complete separation of input, drop and through ports without the need for optical circulators. Photonic crystal (PhC) nanobeam cavities [2] support tight optical mode confinement that promises high efficiency passive and active photonic devices, but their use in an add/drop filter is non-trivial due to the inability of a standing-wave resonator to separate input, through and drop ports. Wavelength filtering has been demonstrated in PhCs [3, 4], but previous approaches have had the traditional limitation of standing-wave resonators that through-port transmission is in reflection and requires a circulator, making these schemes impractical for cascaded WDM channel add-drop filters and wavelength multiplexing. Over 15 years ago, "push-pull" schemes were proposed by Manolatou et al. [5] that enable pairs of standing-wave resonators to emulate the operation of a traveling cavity, but to date we are not aware of a demonstration of this concept.

In this paper, we demonstrate an efficient channel add-drop filter based on a pair of photonic crystal nanobeam cavities, demonstrating for the first time a high-performance 4-port PhC standing-wave resonator based filter directly integrable into an on-chip WDM scheme without any magneto-optic components. The filter has 1 dB insertion loss and 16 dB through port extinction for a 3 dB bandwidth of 64 GHz. We demonstrate the device in an unmodified 45 nm SOI CMOS process, on a chip fabricated in a commercial microelectronics foundry [1, 6]. This work thus lays the groundwork for greater utilization of photonic crystal devices in complex photonic chips. The cavities are not tuned, and the fidelity of the process is shown to be high enough to enable degenerate operation of the cavity pair.

Fig. 1(a) shows the device topology. Two degenerate photonic crystal nanobeams are indirectly coupled via two evanescently-coupled buses. ϕ_1 and ϕ_2 are the optical phase delays in the two connecting paths between the two



Fig. 1. (a) Topology of device; (b) Cross-section of cavity in IBM 45 nm 12SOI CMOS (see PDK [8]); (c) Relative phase offset of about $3\pi/4$ realized with a sinusoid waveguide; (d) 3D rendering of device mask-set layout.



Fig. 2. (a) Optical micrographs of fabricated device from the front and (b) back of chip (substrate removed); (c) Power transmission spectra in each port of the device showing a through-port extinction of 16 dB and a drop loss of 1 dB.

cavities' symmetry planes. The advantage of this topology is that when ϕ_1 and ϕ_2 are engineered correctly, destructive interference occurs in one of the drop ports and only a single drop port or the through port will have non-zero transmission. This allows for one of the drop ports to have near 100% transmission on-resonance. In a single evanescently coupled photonic crystal cavity, all four ports will have non-zero transmission on-resonance, allowing for a maximum of 25% from any single drop port owing to symmetry restrictions. The phases ϕ_1 and ϕ_2 are set so that the symmetric and anti-symmetric supermodes of the device are degenerate. For a device with no direct coupling between the cavities and equal coupling from the top and bottom buses, this occurs when $\cos(\phi_1) = \cos(\phi_2) = 0$ and $\sin(\phi_1) + \sin(\phi_2) = 0$ [5] and thus both the absolute and relative phases of the paths are important. The left drop port is the active drop port when this condition is met.

The cross-section of the device within the IBM 12SOI process is illustrated in Fig. 1(b). Using previous designs of photonic crystal microcavities [7], two cavities were cascaded. A sinusoidal waveguide on the top path was used to bias the relative phase between the top and bottom paths [Fig. 1(c)]. The additional phase gained in the top arm is near $3\pi/4$ for wavelengths in the interval of 1500 nm to 1580 nm. Fig. 1(d) shows a 3D rendering of the device. Two heaters implemented in the crystalline silicon layer (the active layer for transistors) are placed next to each path. This is to bring both paths to the correct absolute phases and to fine tune the relative phase between the two paths.

Fig. 2(a) is a top-view optical micrograph of a 3×3 mm die from a 300 mm, 45 nm node SOI CMOS wafer, and a zoom in view showing grating coupler access ports to the device (not visible, under metal density fill) and heater driving pads for driving probes. Fig. 2(b) is a bottom-view optical micrograph of a fabricated device (grating couplers not shown). Fig. 2(c) shows the response of the device near the degeneracy condition after ϕ_1 and ϕ_2 were tuned. A total electrical power of 13.2 mW was used to power the heaters. On-resonance, the device shows a through-port extinction of 16 dB and an insertion loss of 1 dB through the left drop port. Transmission to the right drop port is below -13.6 dB, showing successful isolation of that port over the operational wavelength range. A bandwidth of 64 GHz (a total Q of 3,020) is measured.

The demonstration of cascaded photonic crystal standing-wave microcavities with a traveling-wave cavity (ring resonator) like response enables photonic crystals to be used in an add-drop filter configuration with low insertion loss and large extinction in monolithic CMOS photonic circuits. A remaining challenge preventing wide adoption of such devices is the complex implementation. A simplified implementation of the same concept, with fewer phase adjustments necessary, could enable wider adoption of PhC devices in photonic chips for WDM applications. This work was supported by DARPA POEM program award HR0011-11-C-0100.

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